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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,541	09/06/2000	William F. Beausoleil	POU9-2000-0047-US1	9916

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ORRICK, HERRINGTON & SUTCLIFFE, LLP
4 PARK PLAZA
SUITE 1600
IRVINE, CA 92614-2558

EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	8

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/656,541	BEAUSOLEIL ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Introduction

1. Claims 1-6 of U.S. Application 09/656,541 filed on 09/06/2000 are presented for examination.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,618,698 in view of Official Notice.

   Independent Claim 1 of U.S. Patent No. 6,618,698 claims a "software-driven multiprocessor emulation system", where "each emulation processor contain[s] an execution unit ... and bus means ... [and] an embedded control

store ... [and] an embedded data store in each of the emulation processors to receive input for, and data generated by the same emulation processor ...".

Dependent Claim 2 of U.S. Patent No. 6,618,698 further claims: "The method according to claim 1, wherein for each emulation step, an emulation processor reads a logic function and associated operands from the data store, performs the operation, and writes the results with an effective speed of the emulation ..."

Dependent Claim 3 of U.S. Patent No. 6,618,698 further claims: "The method according to claim 2, wherein for each cluster, a single emulation step includes reading from the data store (which contains both input data and generated data), setting up the operation, performing the evaluation, and storing the results as an intermediate value, and feeding said intermediate value from one processor to the next processor of a cluster, such that the setup and storing of results is done in parallel with the output of one emulation processor connected to the input of the next emulation processor with said cascade connection providing access to the intermediate values."

Claims 1-3 of U.S. Patent No. 6,618,698 are a functional equivalent to the methods claimed in claims 1 and 2 of the instant application. However, while U.S. Patent No. 6,618,698 teaches "an embedded data store in each of the emulation processors", it does not expressly teach that the "data store" is an SDRAM.

Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an SDRAM as the

"embedded data store", because SDRAMs were well-known and commonly used data storage devices.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The prior art used for these rejections is as follows:

6. Beausoleil et al., U.S. Patent 6,618,698 (Henceforth referred to as "**Beausoleil**").

7. **Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,618,698 ("Beausoleil") in view of Official Notice.**

8. Beausoleil teaches the following limitations of Claim 1:

> Claim 1. In a software driven emulator comprised of a plurality of modules on printed circuit boards, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:
> (Beausoleil, especially: Figures 1-4, col.2, line 20 to col.3, line 35)
>
> transferring data **to** said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;
> (Beausoleil, especially: col.4, line 30 to col.5, line 15)
>
> halting the transfer of data after said predetermined number of data transfers;
> (Beausoleil, especially: col.4, line 30 to col.5, line 15)

However, while Beausoleil does teach that a "bus connected to the multiplexors enables an output from any emulation processor to be transferred to an input of any other of the emulation processors" (see col.3, lines 21-25), Beausoleil does not expressly teach the term "maintenance bus".

Moreover, Beausoleil does not expressly teach the following limitations:

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

In addition, while Beausoleil teaches that "This setup includes routing of the data through multiple evaluation units for the evaluation phase. (For most efficient operation, the input stack and data stack of each processor must be stored in shared memory within each cluster.)", Beausoleil does not expressly teach that each module includes an SDRAM (memory chip) coupled to the processor chip.

In regards to the term "maintenance bus", examiner interprets that it is functionally equivalent to the bus taught in Beausoleil.

In regards to the following limitations:

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

While Beausoleil does not expressly teach these limitation, Beausoleil does teach that "This sum, D1+D2+D3+D4, includes reading from the data store, setting up the operation, performing the evaluation, and storing the results. Note

that setup can include gathering data from other processors on the same module or other modules. We determined that for our planned interconnection networks, the setup times dominate the sum; there is a large differential between the amount of time spent during the setup versus the amount of time spent during the logic evaluation." (see col.4, lines 36-45). Inherent in this teaching is that this time period represents only one cycle, and that the cycle of "reading from the data store, setting up the operation, performing the evaluation, and storing the results" can be repeated.

In regards to the SDRAM coupled to the processor chip, Beausoleil teaches that "the most efficient operation" is with shared memory. This implies that separate memory is also possible, but less efficient. In regards to the use of SDRAM as the memory chip, Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an SDRAM as the "embedded data store", because SDRAMs were well-known and commonly used data storage devices.

9. Beausoleil teaches the following limitations of Claim 2:

Claim 2. In a software driven emulator comprised of a plurality of modules on printed circuit boards, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:
(Beausoleil, especially: Figures 1-4, col.2, line 20 to col.3, line 35)

transferring data **from** said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;
(Beausoleil, especially: col.4, line 30 to col.5, line 15)

halting the transfer of data after said predetermined number of data transfers;
(Beausoleil, especially: col.4, line 30 to col.5, line 15)

However, while Beausoleil does teach that a "bus connected to the multiplexors enables an output from any emulation processor to be transferred to an input of any other of the emulation processors" (see col.3, lines 21-25), Beausoleil does not expressly teach the term "maintenance bus".

Moreover, Beausoleil does not expressly teach the following limitations:

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

In addition, while Beausoleil teaches that "This setup includes routing of the data through multiple evaluation units for the evaluation phase. (For most efficient operation, the input stack and data stack of each processor must be stored in shared memory within each cluster.)", Beausoleil does not expressly teach that each module includes an SDRAM (memory chip) coupled to the processor chip.

In regards to the term "maintenance bus", examiner interprets that it is functionally equivalent to the bus taught in Beausoleil.

In regards to the following limitations:

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

While Beausoleil does not expressly teach these limitation, Beausoleil does teach that "This sum, D1+D2+D3+D4, includes reading from the data store, setting up the operation, performing the evaluation, and storing the results. Note that setup can include gathering data from other processors on the same module or other modules. We determined that for our planned interconnection networks, the setup times dominate the sum; there is a large differential between the amount of time spent during the setup versus the amount of time spent during the logic evaluation." (see col.4, lines 36-45). Inherent in this teaching is that this time period represents only one cycle, and that the cycle of "reading from the data store, setting up the operation, performing the evaluation, and storing the results" can be repeated.

In regards to the SDRAM coupled to the processor chip, Beausoleil teaches that "the most efficient operation" is with shared memory. This implies that separate memory is also possible, but less efficient. In regards to the use of SDRAM as the memory chip, Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an SDRAM as the "embedded data store", because SDRAMs were well-known and commonly used data storage devices.

10. Beausoleil teaches the following limitations of Claim 3:

Claim 3. A method of executing bulk transfers as in claim 1 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.
(Beausoleil, especially: Figs.1-3, "data store", and col.1, line 64 – col.2, line 17)

11. Beausoleil teaches the following limitations of Claim 4:

Claim 4. A method of executing bulk transfers as in claim 2 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.
(Beausoleil, especially: Figs.1-3, "data store", and col.1, line 64 – col.2, line 17)

12. Beausoleil teaches the following limitations of Claim 5:

Claim 5. A method of executing bulk transfers as in claim 1 wherein a data word is transferred on each clock cycle.
(Beausoleil, especially: col.4, lines 36-45)

13. Beausoleil teaches the following limitations of Claim 6:

Claim 6. A method of executing bulk transfers as in claim 2 wherein a data word is transferred on each clock cycle.
(Beausoleil, especially: col.4, lines 36-45)

Conclusion

14. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

15. Beausoleil et al., U.S. Patent 6,051,030.

16. Beausoleil et al., U.S. Patent 4,087,794.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

All communications: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

December 4, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER